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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/564,582
Filing Date: January 12, 2006
Appellant(s): DETECHEVERRY ET AL.

Robert J. Crawford
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 14 December 2009 appealing from the Office action mailed 22 July 2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

The summary of claimed subject matter contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6489663	Ballantine	12-2002
6730983	Minami	5-2004
6693315	Kuroda et al.	2-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3, 5-7, 9 and 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine et al. [6489663] in view of Minami [6730983].

Regarding claims 1 and 22, Ballantine discloses a substrate 12 having a first major surface, an inductive element 16 fabricated on the first major surface of the substrate 12, the inductive element 16 comprising at least one conductive line, a plurality of conducting vias (tilling) structures (30, 32) in at least one layer, wherein the plurality of conducting vias (tilling) structures (30, 32) are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the conducting vias (tilling) structures by a current in the inductive element 16 [Col. 6, Lines 13-33, Figures 1 and 2].

Ballantine discloses the instant claimed invention discussed above except for the conducting vias mentioned as tilling structures.

Minami discloses studs 12 as dummy or tilling structures. Minami further disclose that the plurality of dummy structures arranged to improve manufacturability of semiconductor device [Col. 4, Lines 1-15, Figures 1and 2] and [Col. 2, Lines 1-20].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy structures as taught by Minami to the device of Ballantine.

The motivation would have been to suppress dishing due to CMP and maintain the Q-value of the inductor to a large value [Col. 4, Lines 5-15].

With respect to claim 22, the claim is rejected for reciting method/steps derived from the structure of the rejected claim 1 above.

Regarding claim 2, Minami discloses the tilling structures 12 being made from tilling structure material, wherein the plurality of tilling structures 12 are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element (5, 7) is smaller than the amount of tilling structure material in an area farther away from the inductive element (5, 7) [see Figures 1 and 2].

Regarding claim 3, Ballantine discloses the conducting vias structures (30, 32) are located at different layers, each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the conducting vias structures by a current in the inductive element 16 [Col. 6, Lines 13-33, Figures 1 and 2].

Ballantine discloses the instant claimed invention discussed above except for the conducting vias be mentioned as tilling structures and the structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics.

Minami discloses studs 12 as dummy or tilling structures. Minami further disclose that the plurality of dummy structure is determined by a desired pattern density of the semiconductor device for improving uniformity of Chemical Mechanical Polishing removal rate [Col. 4, Lines 1-15, Figures 1and 2].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy structures as taught by Minami to the device of Ballantine.

The motivation would have been to suppress dishing due to CMP and maintain the Q-value of the inductor to a large value [Col. 4, Lines 5-15].

Regarding claim 5, Ballantine discloses the conducting vias (tilling) structures (30, 32) at different layers are electrically connected to each other [Col. 6, Lines 13-33, Figure 2].

Regarding claim 6, Ballantine discloses the conducting vias (tilling) structures (30, 32) are connected to a DC potential (through 26) [Col. 5, Lines 65-67, Figure 2].

Ballantine further discloses the tilling structures (30, 32) of geometrical pattern that does not substantially inhibit inductive coupling between the inductive element 16 and the substrate 12 [Col. 5, Lines 9-25].

Regarding claim 7, Ballantine discloses the conducting vias (tilling) structures (30, 32) are a plurality of slender elongate elements [Col. 5, Lines 65-67, Figure 1].

Ballantine further discloses the tilling structures (30, 32) of geometrical pattern that does not substantially block penetration into the substrate 12 of electric field lines generated by the inductive element 16 [Col. 5, Lines 9-25].

Regarding claim 9, Ballantine discloses the tilling structures (30, 32) are locally oriented perpendicular to the at least one conductive line of the inductive element 16 [see Figure 1].

Regarding claim 11, Ballantine discloses a ground shield 26 for shielding the inductive element 16 from a further layer [Col. 5, Lines 65-67, Figure 2].

Regarding claim 12, Ballantine discloses the further layer is the substrate 12 [Col. 5, Lines 31-67, Figure 2].

Regarding claim 13, Ballantine discloses connection means electrically connecting the plurality of conducting vias (tilling) structures (30, 32) with the ground shield 26 without creating a conductive loop [Col. 5, Lines 31-67, Figure 2].

Regarding claim 14, Minami discloses the tilling structures 12 are formed in a region other than a region directly below the inductive element (5, 7) [Col. 4, Lines 1-15, Figures 1and 2].

Regarding claims 15 and 16, Ballantine discloses a passive element, which is a capacitive element [Col. 5, Lines 31-55].

Regarding claim 17, Ballantine discloses the capacitive element comprises two capacitor electrodes at least one of the capacitor electrodes being formed by a plurality of conducting vias (tilling) structures (30, 32) [Col. 5, Lines 31-60].

Regarding claim 18, Ballantine discloses a capacitor electrode formed by a plurality of conducting vias (tilling) structures (30, 32) leads to a metal or polysilicon region density in the inductor vicinity respecting the design rules of advanced IC technologies [Col. 5, Lines 17-30].

Regarding claim 19, Ballantine discloses one capacitor electrode of the capacitive element is formed by the ground shield 26 [Col. 5, Lines 16-55].

Regarding claim 20, Ballantine discloses the integration of the capacitive element with the inductive element 14b is optimized to respect the metal pattern density in advanced silicon technologies [Col. 5, Lines 16-55].

Regarding claim 21, Ballantine discloses the distance between the capacitive element and the inductive element 16 is large enough to avoid a dominant fringe coupling between them [Col. 5, Lines 16-65].

Claims 4, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine in view of Minami as applied to claim1 above, and further in view of Kuroda et al. [6693315].

Ballantine in view of Minami discloses the instant claimed invention discussed above except for the tilling structures are plurality of substantially triangular elements.

Kuroda discloses dummy structures are substantially triangular elements [Col. 17, Lines 33-39].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use triangular shape dummy pattern as taught by Kuroda to the structure of Ballantine in view of Minami.

The motivation would have been to provide flatness of the member surface embedded regardless of the shape of the dummy pattern [Col. 14, Lines 40-45].

Regarding claim 10, Ballantine discloses the elements of the conducting vias (tilling) structures are locally oriented perpendicular to the at least one conductive line of the inductive element 16 [see Figure 1].

Regarding claim 4, Ballantine in view of Minami discloses the instant claimed invention discussed above including dummy patterns in different layers except for the geometrical pattern of tilling structures at two different layers is different in shape.

Kuroda discloses geometrical pattern of dummy structures can be of any shape [Col. 17, Lines 33-39].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy patterns of different shape as taught by Kuroda to the different layer of Ballantine in view of Minami.

The motivation would have been to provide flatness of the member surface embedded regardless of the shape of the dummy pattern [Col. 14, Lines 40-45].

(10) Response to Argument

Applicant's arguments with respect to claims 1-22 have been considered but are not persuasive.

Appellant argues (A.1., A.2., pages 4-6) that §103(a) rejection of claims1-3, 5-7, 9 and 11-22 is improper because the cited references Ballantine [U.S. Patent No.6489663] in view of Minami [U.S. Patent No. 6730983] fail to disclose the tilling structures arranged in a geometric pattern substantially inhibit the inducement of an image current in the tilling structures. The Examiner disagrees.

Claim 1 of the Appellant recites "…an inductive element fabricated on the first major surface of the substrate the inductive element comprising at least one conductive line,

a plurality of tilling structures in at least one layer, the plurality of tilling structures arranged to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element."

Vias 28 of the reference Ballantine, which the Examiner asserts as tilling structures, are arranged perpendicularly on rows of ground strips 26 and have the vias one end connected commonly on the ground strip. This configuration inhibits the inducement of an image current from an inductive element. The current is directed to the grounding strip [see Col. 5, Lines 9-16] and [Col. 6, Lines 59-64 of Ballantine].

Column 5, lines 13-16 of Ballantine states, *"This orientation efficiently places conducting **vias 28** in a position **to intercept and terminate** the electric field emanating from spiral inductor 16."*

Column 6, lines 59-64 of Ballantine states, *"The ground plane is cut into a plurality of ground strips in order to prevent the flow of image current that would be induced in a solid ground plane by the magnetic field of the inductor. The ground strips are linked to the inductor by multiple connecting posts called* ***conducting vias****.*

The whole of column 2 of Ballantine further discloses about elimination of image current caused by inductors in semiconductor device.

Appellant argues (A.3., page 7) that the § 103(a) rejection of claims 6 and 7 is improper because the cited references fail to disclose tilling structures do not block penetration into the substrate of electric field lines generated by an inductor. The Examiner disagrees.

Column 5, lines 13-16 of Ballantine as has already been mentioned above, *"This orientation efficiently places conducting vias 28 in a position to intercept and terminate the electric field emanating from spiral inductor 16."*

Therefore, the vias 28 intercepts or blocks the electric field emanating from inductor 16 to avoid penetration into the substrate 12.

Ballantine did not mention the term "tilling structure" in the disclosure, but in column 6, lines 1-55 discussed about the formation of the conductive vias. Ballantine discloses the process the vias are not separately-manufactured components of the integrated circuit but naturally integrated pieces of the device that are created in the normal flow of the manufacturing process [Col. 6, Lines 50-55]. The vias are useful structure in planarazing the resulting surface in the

process using for example, the well known chemical-mechanical polish procedure or CMP. This is the same process the Applicant applies in his invention indicated by tilling structures, which helps in planarazing the resulting surfaces in CMP process [page 1, line 26 of the Specification]. Tilling structures are also disclosed by the Appellant in page 3, paragraph 1 of the Appeal Brief.

The Minami reference is further used in the office action to show a well-known use of **protruding structures** (via-like structure) called **dummy structure** or **tilling structures** are commonly used in semiconductor device with spiral inductor. Minami discloses a spiral inductor 10 has dummy elements 12 arranged on the surface of a substrate. The spiral structure with such a structure is possible to decrease the coupling of the spiral conductor with the substrate while suppressing dishing (uneven surface) due to the CMP [Col. 4, Lines 5-14, Figures 1 and 2]. Ballantine as discussed above has disclosed this matter in the form vias which are not separately-manufactured components.

Appellant argues (A.4., page 8) that the §103(a) rejection of claims 17-19 is improper because the cited references fail to disclose a device that includes an inductive element, tilling structures and capacitive element.

Appellant argue that the reference Ballantine do not teach that vias 28 form one of the electrode of a capacitive element and that ground strip 26 form another electrode of the capacitive element. The Examiner disagrees.

As what the Appellant has mentioned the vias 28 decreases the parasitic capacitance present between the inductor 16 and ground strip 26 referring to column 5, lines 40-45 of Ballantine.

Claims 17-19 requires the semiconductor device provide a capacitive element being formed by a plurality of tilling structures and ground shield. As disclosed by Ballantine, vias 28 and ground shield 26 decreases parasitic capacitance with the inductor 16. The ground strips are capacitively linked to the inductor by multiple conducting vias [Col. 4, Lines 36-54]. Therefore, there is a capacitive element that exist in the semiconductor device structure taught by Ballantine.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joselito Baisa

/J. B./

Examiner, Art Unit 2832

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